QSFP-100G-LR4-AR-LEG
ARISTA NETWORKS 100GBASE-LR4 QSFP28 SMF
WDM 10KM REACH LC DOM

QSFP-100G-LR4-AR-LEG
100Gbase-LR4 QSFP28 Transceiver

Features

- Hot pluggable QSFP28 MSA form factor
- Compliant to IEEE 802.3ba 100GBase-LR4
- Up to 10km reach for G.652 SMF
- Single +3.3V power supply
- Operating caste temperature: 0~70°C
- Transmitter: cooled 4x25Gb/s LAN WDM EML TOSA (1295.56, 1300.05, 1304.58, 1309.14nm)
- Receiver: 4x25Gb/s PIN ROSA
- 4x28G Electrical Serial Interface (CEI-28G-VSR)
- Maximum power consumption 4.0W
- Duplex LC receptacle
- RoHS-6 compliant

Applications

- 100GBase-LR4 Ethernet Links
- Infiniband QDR and DDR interconnects
- Client-side 100G Telecom connections

Product Description

Legrand's QSFP-100G-LR4-AR-LEG Quad Small Form Factor Pluggable (QSFP28) transceivers are compatible with the Small Form Factor Pluggable Multi-Sourcing Agreement (MSA). The QSFP28 transceivers are high performance, cost effective modules supporting 100 Gigabit Ethernet and up to 10km transmission distance with SMF.

Legrand's QSFP28 transceivers are RoHS compliant and lead-free.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	-0.5		3.6	V
Damage Threshold, each Lane	THd	5.5			dBm
Storage Temperature	Tst	-40		85	°C
Case Operating Temperature	Top	0		70	°C
Humidity (non-condensing)	Rh	5		85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tca	0		70	°C
Data Rate Per Lane	fd		25.78125		Gbps
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low	Pm	0		0.5	V
Link Distance with G.652	D			10	km

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Consumption				4.0	W	
Supply Current	Icc			1.21	A	
Transceiver Power-on Initialization Time				2000	ms	1
Transmitter						
Single-ended Input Voltage Tolerance		-0.3		4.0	V	2
AC Common Mode Input Voltage Tolerance		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	Vin,pp	190		700	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Receiver						
Single-ended Output Voltage		-0.3		4.0	V	
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	Vout,pp	300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	ohm	

Note:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range o the instantaneous input signals.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09		
	L2	1303.54	1304.58	1305.63		
	L3	1308.09	1309.14	1310.19		
Transmitter						
RMSR	SMSR	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-4.3		4.5	dBm	
OMA, each Lane	P_{OMA}	-1.3		4.5	dBm	
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-2.3			dBm	
TDP, each Lane	TDP			2.2	dB	
Extinction Ratio	ER	4			dB	
$RIN_{20}OMA$	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Eye Mask Coordinates: X1, X2, X3, Y1, Y2, Y3	Specification Values 0.25, 0.4, 0.45, 0.25, 0.28, 0.4					2
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Damage Threshold, each Lane	TH_d	5.5			dBm	3

Total Average Receive Power				10.5	dBm	
Average Receive Power, each Lane		10.6		4.5	dBm	
Receiver Power (OMA), each Lane				4.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-8.6	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-6.8	dBm	4
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			5.5	dB	
LOS Assert	LOSA		-18		dBm	
LOS Deassert	LOSD		-15		dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			31	GHz	

Note:

1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. See Figure 1 below.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$
5. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

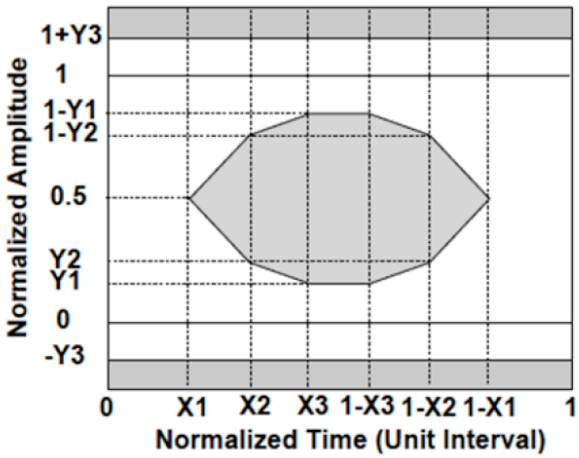


Figure 1. Eye Mask Definition

Pin Descriptions

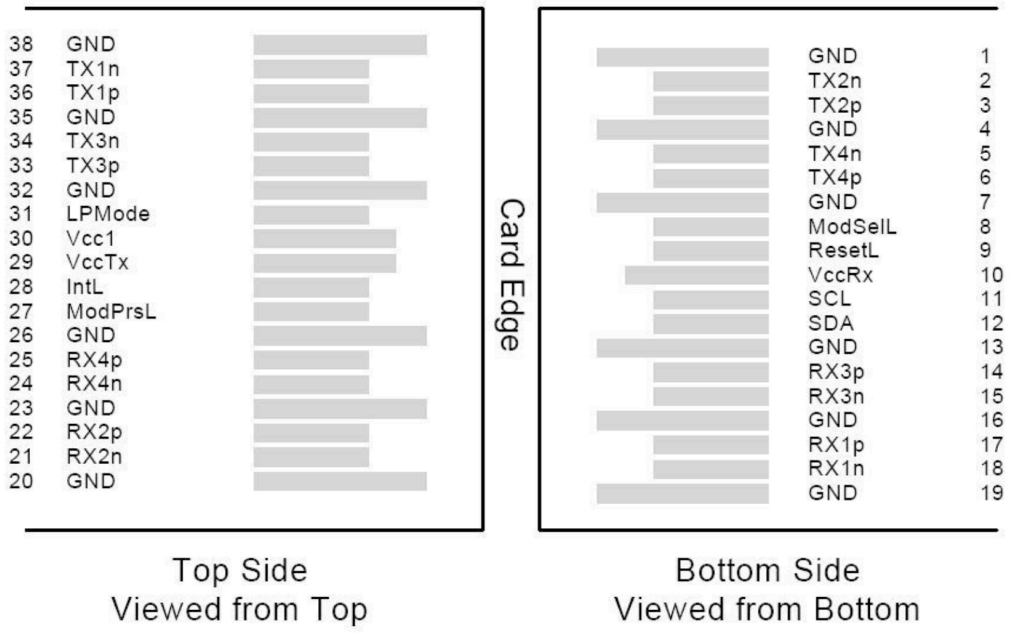
Pin	Logic	Symbol	Name/Descriptions	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted dta output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module Ground	1

33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

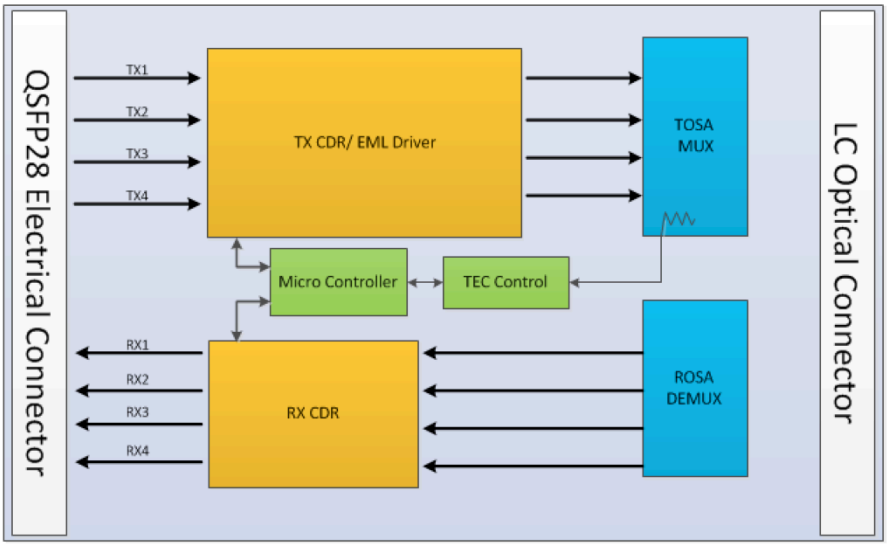
Note:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Electrical Pin-out Details



Transceiver Block Diagram



Mechanical Specifications

Measurement unit: mm