FTLC1121RDNL-LEG
FINISAR 100GBASE-LR4 CFP2 SMF
1310nm 10KM REACH LC DOM

FTLC1121RDNL-LEG
100Gbase CFP Transceiver

Features

- Operating optical data rate up to 112Gbps
- Transmission distance up to 10km
- CFP MSA compliant
- Compliant to 100GbE IEEE 802.3ba specification for 100GBASE-LR4
- OTU4 compatible
- 1310 nm window cooled EA-DFB LD and PIN ROSA
- Built in digital diagnostic function
- 10 parallel electrical serial interface and AC coupling of CML signals
- Hot pluggable electrical interface
- Lower power dissipation <16W
- Operating case temperature 0°C to +70°C
- Single 3.3V power supply
- RoHS 6 compliant (lead free)

Product Description

Legrand's FTLC1121RDNL-LEG Form Factor Pluggable CFP transceivers are compatible with the Small Form Factor Pluggable Multi-Sourcing Agreement (MSA). The CFP transceivers are high performance, cost effective modules supporting 100 Gigabit Ethernet and up to 10km transmission distance with SMF.

Legrand's CFP transceivers are RoHS compliant and lead-free.

Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>500 V) Isolation with the case
Electromagnetic Interference (EMI)	FCC Part 15 Class B	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compatible with Class I laser product. Compatible with TμV standards
Component Recognition	UL and CUL	UL file E317337
Green Products	RoHS	RoHS6

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TST	-40	+85	°C
Supply Voltage	VCC	-0.5	3.6	V
Operating Case Temperature Range	Tc	-5	75	°C
Humidity (non-condensing)	Rh	5	85	%
Receiver Damage Threshold Per Lane	Pdag	5.5		dBm

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	TOP	0		+70	°C
Power Supply Voltage	VCC	3.2	3.3	3.41	V

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential Input Impedance	Zin	80	100	120	ohm
Frequency		161.1328125/644.53125			MHz
Frequency Stability	Δf	-100		100	ppm
		-20		20	
Output Differential Voltage	VDIFF	400		1200	mV
RMS jitter 1-2	0			10	ps
Clock Duty Cycle		40		60	%
Clock Rise/Fall Time 10%/90%	tr/f	200		1250	Ps
		50		315	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signaling Rate for Each Lane (100GbE)				25.78125	Gbps
Signaling Rate for Each Lane (OTU4)				27.95249	
Transmitter					
Four Lane Wavelength Range	λ1	1294.53	1295.56	1296.59	nm
	λ2	1299.02	1300.05	1301.09	
	λ3	1303.54	1304.58	1305.63	
	λ4	1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	30			dB

Total Average Launch Power	Pt			10.5	dBm
Average Launch Power for Each Lane (100GbE)	Pa	-4.3		4.5	dBm
Average Launch Power for Each Lane (OTU4)		-2.9		4.5	
Optical Modulation Amplitude for Each Lane	OMA	-1.3		4.5	dBm
Transmitter and Dispersion Penalty for Each Lanes				2.2	TBP
Average Launch Power of Off Transmitter for Each Lanes	Poff			-30	dBm
Extinction Ratio (100GbE)	EX	4			dB
Extinction Ratio (OTU4)		7			
RIN20OMA				-130	dB/Hz
Optical Return Loss Tolerance				20	dB
Transmitter Reflectance				-12	dB
Transmitter eye mask	Compliant to IEEE802.3ba-LR4/OTU4				
Receiver					
Four Lane Wavelength	λ1	1294.52	1295.56	1296.59	nm
	λ2	1299.02	1300.05	1301.09	
	λ3	1303.54	1304.58	1305.63	
	λ4	1308.09	1309.14	1310.19	
Overload Input Optical Power	Pmax	5.5			dBm
Average Receive Power for Each Lane (100GbE)	Pin	-10.6		4.5	dBm
Average Receive Power for Each Lane (OTU4)		-9.2		4.5	
Receive Power In OMA for Each Lane	PinOMA			4.5	dBm
Difference in Receive Power between any two				5.5	dBm
Receiver Sensitivity in OMA for Each	SOMA			-8.6	dBm
Receiver Sensitivity in OMA for Each Lane (OTU4)				-10.8	
Stressed Receiver Sensitivity in OMA for Each				-6.8	dBm
Los Assert				-12	dBm
Los De-assert		-17			dBm
Los Hysteresis				0.2	dBm

Pin Descriptions

Part A: Bottom Row Pin Function Definition

Pin	Symbol	Type	I/O	Description

1	3.3V_GND	GND		3.3V Module Supply Volage Return Ground, Can be separate or tied together with Signal Ground
2	3.3V_GND	GND		
3	3.3V_GND	GND		
4	3.3V_GND	GND		
5	3.3V_GND	GND		
6	3.3V	VCC		3.3V Module Supply
7	3.3V	VCC		
8	3.3V	VCC		
9	3.3V	VCC		
10	3.3V	VCC		
11	3.3V	VCC		
12	3.3V	VCC		
13	3.3V	VCC		
14	3.3V	VCC		
15	3.3V	VCC		
16	3.3V_GND	GND		
17	3.3V_GND	GND		
18	3.3V_GND	GND		
19	3.3V_GND	GND		
20	3.3V_GND	GND		
21	NC		I/O	Do not use
22	NC		I/O	Do not use
23	GND	GND		
24	(TX_MCLKn)	CML	O	Do not use
25	(TX_MCLKp)	CML	O	Do not use
26	GND	GND		
27	NC		I/O	Do not use
28	NC		I/O	Do not use
29	NC		I/O	Do not use
30	PRG_CTL1	LVCMOS	I	Programmable Control 1 set via MDIO, MSA default: TRXIC_RSTn-TX

		w/PU		& RX IC reset. “0”=reset, “1” or NC = enabled or not used
31	PRG_CTL2	LVCMOS w/PU	I	Programmable Control 2 set via MDIO, MSA default: Hardware power Interlock LSB, “00” = <8W, “01” = <16W, “10” < 24W, “11” or NC = >24W or not used
32	PRG_CTL3			Programmable Control 3 set via MDIO, MSA default: Hardware power Interlock MSB, “00” = <8W, “01” = <16W, “10” < 24W, “11” or NC = >24W or not used
33	PRG_ALRM1	LVCMOS	O	Programmable Alarm 1 set via MDIO, Reflex default: HIPWR_ON, Module power on indicator. “1” = Module high power up completed, “0” = Module not high powered up
34	PRG_ALRM2	LVCMOS	O	Programmable Alarm 2 set via MDIO, Reflex default: MOD_READY, module initialization complete, “1” = complete, “0” = not complete
35	PRG_ALRM3	LVCMOS	O	Programmable Alarm 3 set via MDIO, Reflex default: MOD_FAULT, module fault detected, “1” = fault, “0” = no fault
36	TX_DIS	LVCMOS w/PU	I	Transmitter Disable for all channels, “1” or NC = transmitter disabled, “0” = transmitter enabled
37	MOD_LOPW	LVCMOS w/PU	I	Module low power mode. “1” or NC = module in low power (safe) mode, “0” = power-on enabled
38	MOD_ABS	GND	O	Module Absent. “1” or NC = Module absent, “0” = module present. Pull-up resistor on Host
39	MOD_RSTn	LVCMOS w/PD	I	Module Reset. “0” = reset the module, “1” or NC = module enabled, Pull Down resistor in module
40	RX_LOS	LVCMOS	O	Receiver loss of optical signal on any channel, “1” = loss of signal, “0” = normal condition
41	GLB_ALRMn	LVCMOS	O	Global Alarm. “0” = alarm condition in any MDIO alarm register, “1” = no alarm
42	PRTADR4	1.2V CMOS	I	MDIO port address bit 4
43	PRTADR3	1.2V CMOS	I	MDIO port address bit 3
44	PRTADR2	1.2V CMOS	I	MDIO port address bit 2
45	PRTADR1	1.2V CMOS	I	MDIO port address bit 1
46	PRTADR0	1.2V CMOS	I	MDIO port address bit 0
47	MDIO	1.2V CMOS	I/O	Management Data I/O bi-directional data (electrical specs as per 802.3ae)
48	MDO	1.2V CMOS	I	Management data clock (electrical specs as per 802.3ae)
49	GND	GND		
50	NC		I/O	Do not use
51	NC		I/O	Do not use
52	GND	GND		
53	NC		I/O	Do not use
54	NC		I/O	Do not use
55	3.3V_GND	GND		3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND	GND		

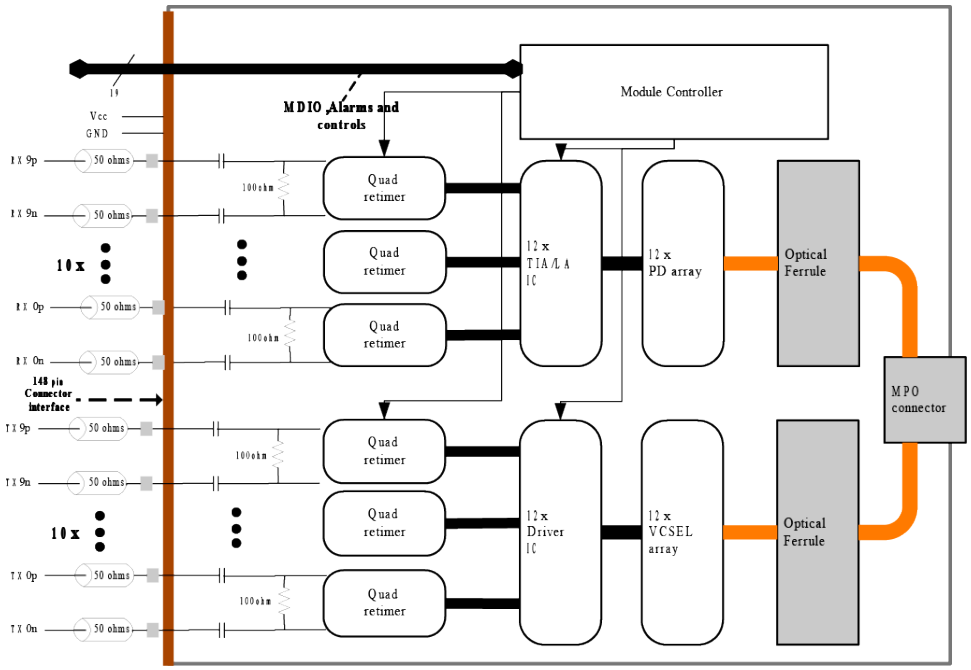
57	3.3V_GND	GND		
58	3.3V_GND	GND		
59	3.3V_GND	GND		
60	3.3V	VCC		3.3V Module Supply
61	3.3V	VCC		
62	3.3V	VCC		
63	3.3V	VCC		
64	3.3V	VCC		
65	3.3V	VCC		
66	3.3V	VCC		
67	3.3V	VCC		
68	3.3V	VCC		
69	3.3V	VCC		
70	3.3V_GND	GND		
71	3.3V_GND	GND		
72	3.3V_GND	GND		
73	3.3V_GND	GND		
74	3.3V_GND	GND		

Part B: Top Row Pin Function Definition

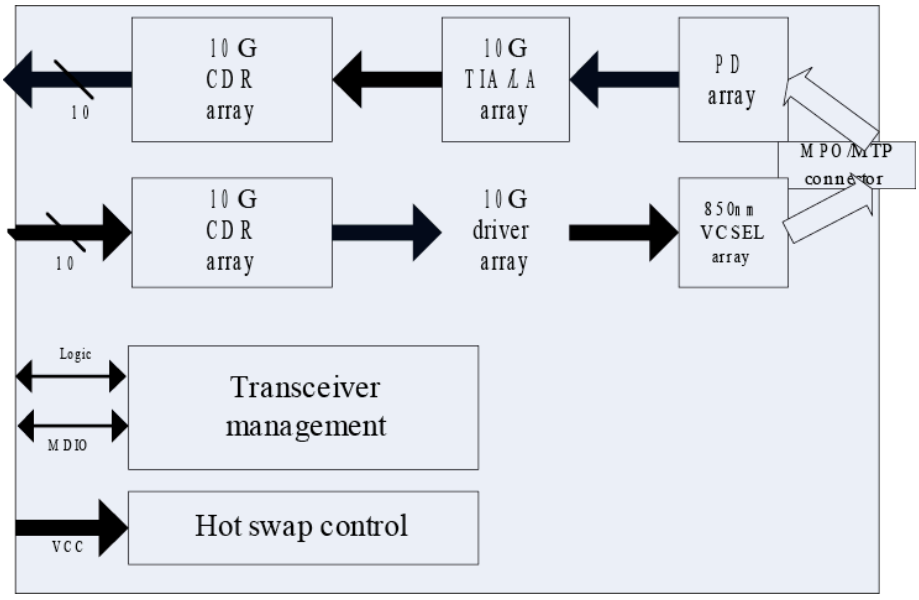
Pin	**Symbol**	**Pin**	**Symbol**	Pin	Symbol	Pin	Symbol	Pin	Symbol
148	GND	136	GND	124	GND	112	GND	100	RX7p
147	Not used	135	TX7n	123	TX3n	111	GND	99	GND
146	Not used	134	TX7p	122	TX3p	110	Not used	98	RX6n
145	GND	133	GND	121	GND	109	Not used	97	RX6p
144	Not used	132	TX6n	120	TX2n	108	GND	96	GND
143	Not used	131	TX6p	119	TX2p	107	RX9n	95	RX5n
142	GND	130	GND	118	GND	106	RX9p	94	RX5p
141	TX9n	129	TX5n	117	TX1n	105	GND	93	GND
140	TX9p	128	TX5p	116	TX1p	104	RX8n	92	RX4n

139	GND	127	GND	115	GND	103	RX8p	91	RX4p
138	TX8n	126	TX4n	114	TX0n	102	GND	90	GND
137	TX8p	125	TX4p	113	TX0p	101	RX7n	89	RX3n
88	RX3p	85	RX2p	82	RX1p	79	RX0p	76	Not used
87	GND	84	GND	81	GND	78	GND	75	GND
86	RX2n	83	RX1n	80	RX0n	77	Not used		

CFP Module Functional Block Diagram



Module Block Diagram



Mechanical Specifications